NAND/NOR Implementation of Logic Functions

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EECS: 1100 Digital Logic Design
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Lab Assignment #6

1. Objectives

- implementing logic functions expressed in nonstandard form,
- deriving all-NAND implementation of multilevel logic circuits,
- deriving the sum of minterms *canonical form* of Boolean functions,
- becoming acquainted with the BCD to seven segment decoder ICs and the seven segment display components,
- developing skills in designing and testing combinational logic circuits.
- improving the proficiency in using sophisticated equipment.

2. Prelab Assignment

2.1 ALL-NAND IMPLEMENTATION OF MULTILEVEL LOGIC CIRCUITS

Algebraic form of a logic function Y(E,D,C,B,A) is given as equation (2.1-1),

$$Y(E,D,C,B,A)= (A\cdot B+C)\cdot D+E \qquad (2.1\text{-}1)$$

2.1.1 Prepare a truth table of the function Y, and show it as Table T2.1-1.

Hint#1 To avoid unnecessary loss of time while completing the assignment of Section 4.1 below, remember that the designation Y(E,D,C,B,A) implies that the list of variables in the truth table of the function is in the order E,D,C,B,A.

2.1.2 Prepare a logic circuit representation/implementation of the nonstandard expression (2.1-1) of the function Y, and show the logic circuit diagram as Figure 2.1-1.

2.1.3 Design an all-NAND implementation of the logic circuit shown in Figure 2.1-1 and show it as Figure 2.1-2(a).

2.1.4 Design an all-NOR implementation of the logic circuit shown in Figure 2.1-1 and show it as Figure 2.1-3.

2.1.5 Compare logic circuit implementations of the function Y which are shown in Figures 2.1-2(a) and 2.1-3. Which one of the two has more logic gate time delays in the path of signal A?

2.1.6 Using integrated circuit components listed in section 3.2, design a physical layout of the logic circuit shown in Figure 2.1-2(a). Show a computer generated drawing of the designed layout as Figure 2.1-2(b). Provide IC package pinouts in all drawings of Figure 2.1-2.

Hint#2 Pinouts (pin numbers) are available in Figure 2.5 of the course text book, pp.107-109, and in the TTL Data Book.

2.2 BCD TO SEVEN SEGMENT DECODING AND DISPLAY

Figure A.4-2 shows a connection of the IC 7448, the BCD-to-7-segment decoder, and the 7-segment LED display component. The shown connection of those two components is commonly used for displaying a decimal representation of the BCD encoded numerical data. In the circuit of Figure A.4-2 the source of the BCD encoded data is a decade counter, which is implemented by the 7493 ripple counter whose inputs R1 and R2 are connected as shown in Figure A.4-2.

2.2.1 Design a physical layout of the logic circuit shown in Figure A.4-2. Show a computer generated drawing of the designed layout as Figure 2.2-1. Provide the IC and 7-segment display package pinouts in the drawing.

Hint#3 Pinouts (pin numbers) of both packages are shown in Figure A.4-2.

Hint#4 The current semester Lab experiments will be conducted using the 7-segment display component which has its pins arranged along the vertical edges.

2.2.2 Based on the lower-case-letter encoding of the seven segments shown in Figure A.4-2, determine the sequences of letters which designate the segments which should be turned on to display the digits "0", "4", and "8". Show the determined sequences as table T2.2-1.

3. Lab Equipment and Circuit Components

3.1 EQUIPMENT

Equipment to be used includes:

- Proto boards: Global PB-104, or PB-105,
- Agilent E3631A DC power supply,
- Function generator: Agilent 33120A,
- Mixed-Signal oscilloscope Agilent 54645D,
- Dell GxaEM computer system.

3.2 CIRCUIT COMPONENTS

- IC component 7400, quad 2-input NAND gates (1)
- IC component 7404, hex inverters (1)
- IC component 7448, BCD to seven segment (common-cathode) decoder (1)
- IC component 7493, ripple counter (1)
- Common-cathode seven segment display component (1)

4. Lab Experiment

4.1 MULTILEVEL ALL-NAND IMPLEMENTATION

4.1.1 Using the physical layout diagram of Figure 2.2-1(b) as a reference, build on proto board a physical implementation of the logic circuit shown in Figure 2.2-1(a). As an auxiliary logic circuit, build additionally the binary counter which was used in Lab Assignment #1 to generate binary representations of integers 0 through 15. The same circuit is repeated in Figure A.4-1, which shows the complete circuit for experimenting with the multiple level all-NAND implementation of the function Y of equation (2.1-1).

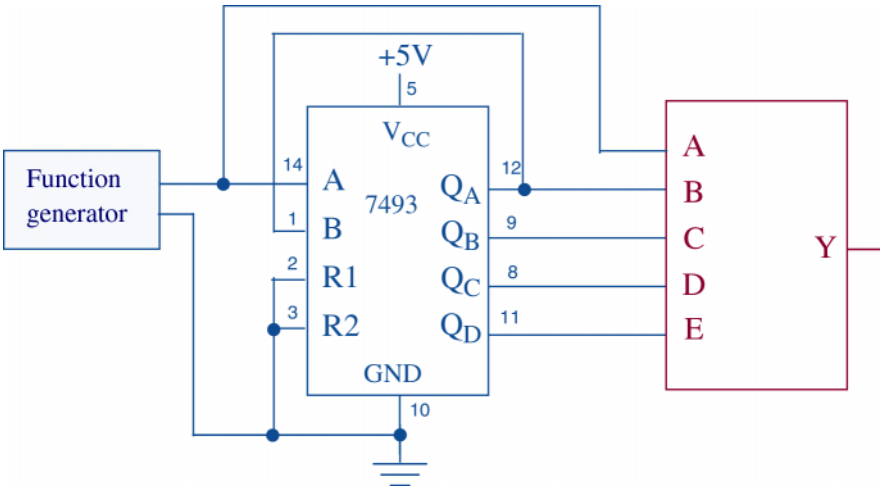


Figure A-4.1 The circuit for experimenting with the implementation of the logic function f, of equation (2.1-1), using a black-box representation of the function's circuit.

4.1.2 Connect digital channels D0 through D5 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.1.1:

- digital channel D0: to the input A of the circuit which implements the function Y,
- digital channel D1: to the input B of the circuit which implements the function Y,
- digital channel D2: to the input C of the circuit which implements the function Y,
- digital channel D3: to the input D of the circuit which implements the function Y,
- digital channel D4: to the input E of the circuit which implements the function Y
- digital channel D5: to the output Y of the circuit which implements the function Y.

Establish a ground connection. Turn on digital channels D0 through D5, and rename the channels D0 through D5 as A,B,C,D,E and Y respectively.

4.1.3 Adjust the frequency of the Agilent 33120A function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 00000 on channels D0 through D4. Hit the key Single on the Agilent 54645D. Adjust the display of

waveforms so that the first appearance of the combination of signal values 00000 on channels D0 through D4 is positioned at the left end of the screen, and that the whole screen shows ten percent more than one period of the signal at the input E.

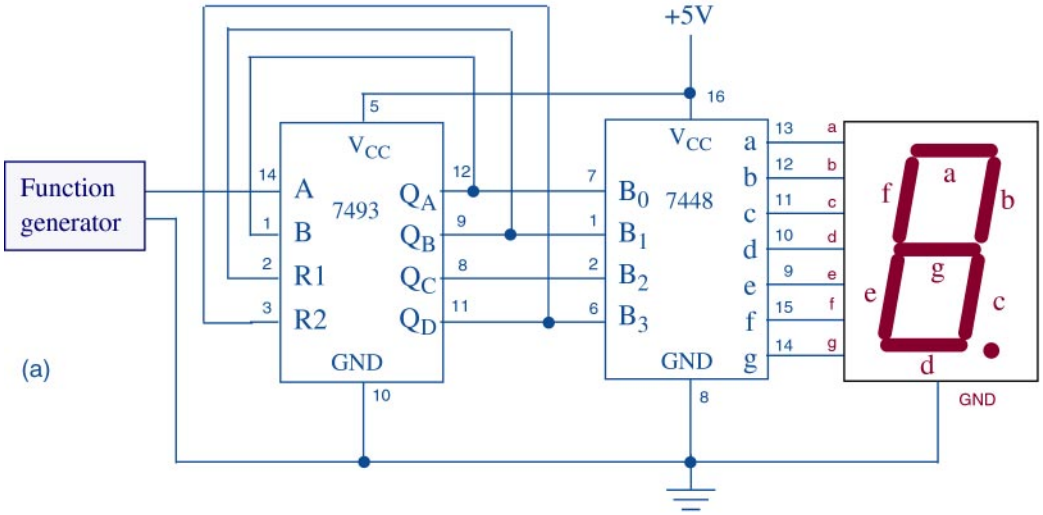
4.1.4 Verify correct functioning of the all-NAND logic circuit implementation of the function Y by comparing the obtained waveforms to the truth table T2.1-1. If the waveforms do not match contents of the truth table, find and correct the error(s).

4.1.5 Save the Screen Image of the correct waveforms of the channels D0 through D5 to a file named L6_415.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.2 BCD TO 7-SEGMENT CODE CONVERSION

4.2.1 Using as a reference the prepared physical circuit diagram from Figure 2-3, build on the proto board the physical circuit in which the seven segment display component will show all ten decimal digits in sequence.

(a)



(b)

pins on vertical edges LSD8151-10	display segment	pins on horizontal edges
1	a	9
14	b	7
12	c	6
10	d	4
4	e	2
2	f	1
13	g	10
9	DPR	5
6	DPL	
3,5,11,16	GND	3,8

Figure A.4-2 Circuit for experimenting with the BCD to 7-segment conversion. (a)Circuit of the arrangement which is used to display one decimal digit of a number in BCD representation. (b) Pinouts of two different packages of common-cathode 7-segment display components.

4.2.2 Adjust the frequency of the Agilent 33120A function generator to 1Hz and observe the seven segment display to verify the correct functioning of the constructed circuit.

4.2.3 Connect digital channels D0 through D6 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.2.1:

- digital channel D0: to the segment a of the 7-segment display,
- digital channel D1: to the segment b of the 7-segment display,
- digital channel D2: to the segment c of the 7-segment display,
- digital channel D3: to the segment d of the 7-segment display,
- digital channel D4: to the segment e of the 7-segment display,
- digital channel D5: to the segment f of the 7-segment display,
- digital channel D6: to the segment g of the 7-segment display.

Establish a ground connection. Turn on digital channels D0 through D6, and rename the channels D0 through D6 as a, b, c, d, e, f, and g respectively.

4.2.4 Adjust the frequency of the function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 1111110 on channels D0 through D6. Hit the key Single on the Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 1111110 on channels D0 through D6 is positioned at the left end of the screen, and that the whole screen shows ten percent more than two sequences of digits 0 through 9.

4.2.5 Save the Screen Image of the correct waveforms of the channels D0 through D5 to a file named L6_426.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.3 TRANSFER OF CAPTURED WAVEFORMS.

Transfer (ftp) the files L6_*.tif from the Dell GxaEM computer system to your personal College of Engineering computer account.

5. Postlab Assignment

5.1 MULTILEVEL ALL-NAND IMPLEMENTATION OF THE FUNCTION Y

5.1.1 Show the waveform stored in the file L6_415.tif as Figure 5.1-1. Mark by vertical red lines in the Figure 5.1-1 the combinations of the input variables for which the function Y has the value of logical one. Using the marked waveforms,

(a) verify the correct functioning of the circuit by comparing marked combinations with the corresponding rows in the truth table T2.1-1;

(b) prepare the expression of the function Y in the sum of minterms canonical form;

(c) compare the numbers of logic gates and of logic gate inputs of the logic circuit which would implement the sum of minterms canonical form as a two-level AND-OR/NAND-NAND circuit, to the corresponding numbers of the logic circuit of Figure 2.1-2(a).

5.2 BCD TO 7-SEGMENT CODE CONVERSION

5.2.1 Show the waveforms stored in the file L6_426.tif as Figure 5.2-1. Mark by vertical red lines in the Figure 5.2-1 the signal combinations that create a display of digits "1", "3", and "9".

6. Lab Report

To be considered complete, the lab report must contain the following,

1. Cover sheet - Lab style, filled out,
2. The truth table, and the logic circuit and physical layout diagrams prepared under 2.1 and 2.2.
3. The waveforms and the sum of minterms expression as prepared under 5.1 and 5.2.
4. A report on items not already included under 1. through 3. above, which includes:
   - a discussion of the insights gained through the conducted experiments,
   - textual description and graphical/ tabular illustration of the design procedure(s),
   - description of implemented testing procedures,
   - conclusions reached as a result of performing the lab experiment,
   - comments and suggestions that might lead to easier and/or deeper understanding of the topics covered by the assignment.